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(54) Camouflaged circuit structure with implants

(57) Connections between implanted regions (34a, 34b) in a semiconductor substrate (36), such as the sources (S1, S2) or drains (D1, D2) of adjacent transistors (T1, T2), are made by buried conductive implants (40) rather than upper level metalizations. The presence or absence of a connection between two implanted regions is camouflaged by implanting a conductive buried layer (40) of the same doping conductivity as the implanted regions when a connection is desired, and a field implant (44) of opposite conductivity to the implanted regions when no connection is desired, and forming steps (46a, 46b) into the substrate at the boundaries of the buried layer or field implant that mask the steps (52a, 52b) formed between different conductivity regions during a selective etch by a reverse engineer. The masking steps are preferably formed by field oxide layers (38) that terminate at the boundaries of the buried layers and field implants.

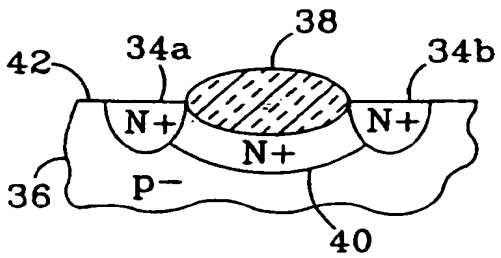

FIG.2a

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Descripti n

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to the prevention of reverse engineering of integrated circuits (ICs), and more particularly to security techniques in which the conductive or nonconductive nature of interconnections between circuit elements is made camouflaged.

Description of the Related Art

Several techniques have been used to reverse engineer ICs. Electron (e)-beam probing with a scanning electron microscope (SEM), either through SEM photographs or voltage contrast analysis, is a standard reverse engineering mechanism, although secondary ion mass spectrometry (SIMS), spreading resistance analysis and various other techniques have also been used. A general description of e-beam probing is provided in Lee, "Engineering a Device for Electron-beam Probing", IEEE Design & Test of Computers, 1989, pages 36-49.

Numerous ways to frustrate unwanted attempts to reverse engineer an IC have also been developed. For example, in Patent No. 4,766,516 to Ozdemir et al. (assigned to Hughes Electronics, the assignee of the present invention), additional circuit elements that do not contribute toward the desired circuit function are added to an IC, and disguised with the visible appearance of being an ordinary part of the IC. The elements have physical modifications that are not readily visible but cause them to function in a different manner, inhibiting the proper functioning of the IC in case of an attempted copying or other unauthorized use. When the apparent function rather than the actual function of the disguised elements is copied, the resulting circuit will not operate properly.

In Patent No. 4,583,011 to Pechar a pseudo-MOS (metal oxide semiconductor) device is given a depletion implant that is not readily visible to a copier, who would infer from the device's location in the circuit that it would be enhancement-mode. A somewhat related approach is taken in French patent publication no. 2 486 717 by Bassett et al., published January 15, 1982; the circuit doping is controlled so that some devices which appear to be transistors actually function as either open or short circuits. And in Patent No. 4,603,381 to Guttag the memory of a central processing unit is programmed by the doping of its channel regions, rather than by the presence or absence of gates, to protect permanently programmed software.

Instead of disguising circuit elements, some systems have a mechanism to protect the circuit from operating until a correct access code has been entered. Such systems are described in Patent Nos. 4,139,864 to Schulman and 4,267,578 to Vetter.

Each of the above protection schemes requires additional processing and/or uses additional circuitry that is dedicated to security and does not contribute to the basic functioning of the circuit. This increases the cost of circuit production and complicates the circuitry.

Patent No. 4,799,096 to Koeppe uses doped implants to connect the sources and drains of different transistors to improve circuit reliability and testability, but the circuit function can be determined from the transistor arrangement. Patent No. 5,138,197 to Kuwana connects different transistors in an address decoder array with doped implants, but circuit functions can be determined from clearly visible elements such as gate electrodes and circuit interconnects. Japanese patent publication 58-190064 to Sawase provides a metalization over a diffused source to block light from the source/substrate junction and thus reduce leakage current. While this tends to camouflage the source, the nature of the circuit can still be determined from its visible elements.

In related application Serial No. 08/532,326, filed September 22, 1995 by the present inventors, heavily doped implant interconnections that are difficult for a reverse engineer to detect are used to provide interconnections among the transistors of various types of logic cells, with the pattern of interconnections determining each cell's logic function. The transistors of the different cells are arranged in a common pattern and a uniform pattern of interconnections among transistors is provided for each cell; different logic functions are implemented by interrupting some of the interconnections with the addition of opposite conductivity channel stop implants. The channel stops are quite small, making the interrupted and thereby non-conductive interconnections appear the same to a reverse engineer as the conductive interconnections. CMOS digital circuits such as NAND and NOR gates are camouflaged so that they appear identical under an optical microscope. However, when all of the device layers on top of the bare semiconductor substrate have been removed by a reverse engineer and an etchant applied to the underlying substrate, the pattern of channel stops may be brought out by selective etching of the substrate. If an etchant is used which etches N and P type material at different rates (typically N-doped material will etch faster than P-doped), a height differential or "step" will be formed at the boundaries between the channel stop and the adjacent oppositely doped interconnection line. If they are large enough, such steps can be detected by either optical microscopes or SEMs, thereby revealing which interconnections have blocking channel stops and which are true conductive interconnections.

SUMMARY OF THE INVENTION

The present invention seeks to provide a camouflaged circuit structure that enjoys the advantages of the

channel stops used in the related application, but is not subject to reverse engineering by selective etching of the substrate surface.

The presence or absence of an electrical connection between two spaced conductive implants having a common conductivity in a semiconductor substrate, such as the implanted sources or drains of a pair of adjacent MOSFETs, is camouflaged by establishing steps relative to the substrate surface at the boundaries of the interconnection area. These intentional steps mask the steps that result from a reverse engineering selective etch, preventing a reverse engineer from using either an optical microscope or a SEM to determine whether steps have been produced by the selective etch.

The intentional steps are preferably formed by having an insulating layer, preferably a field oxide formed by a local oxidation of silicon (LOCOS) process, extend into the substrate above and up to the boundaries of the interconnection area. An electrical connection between the two implants is made with a buried layer immediately below the field oxide having the same conductivity as the spaced implants, while the implants can be isolated from each other by means of a buried layer below the field oxide of opposite conductivity to the implants; the latter buried layer together with the field oxide inhibits current flow between the implants. Thus, while some of the transistors will be connected to each other and other transistors will be isolated from each other, a reverse engineer cannot tell whether or not any two adjacent transistors are actually connected.

The invention is applicable to both N-channel and P-channel devices. In one particular implementation the camouflaged connection/isolation is provided in a central area that extends between the two transistors and is covered with a field oxide, with the areas lateral to the central area provided with isolating implants and no field oxide.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a logic circuit to which the invention is applicable;

FIG. 2a is a sectional view of an IC substrate showing a camouflaged circuit connection between two doped implant regions in accordance with the invention;

FIG. 2b is a sectional view similar to FIG. 2a, but with a camouflaged electrical isolation between the two implant regions;

FIGs. 3a and 3b are sectional views respectively showing the circuit structures of FIGs. 2a and 2b with the top layers removed by a reverse engineer;

FIG. 4 is a plan view of an IC substrate with two CMOS transistor pairs formed in accordance with the invention;

FIG. 5 is a sectional view taken along the section line 5-5 of FIG. 4;

FIG. 6 is a sectional view taken along the section line 6-6 of FIG. 3 for the case of a camouflaged conductive interconnection between the two transistors;

FIG. 7 and 8 are sectional views taken along the section lines 7-7 and 8-8, respectively, of FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

Related application Serial No. 08/532,326 camouflages digital logic cells by arranging all of the transistors for each of the cells in a uniform "sea" of transistors in which the boundaries between different cells are not apparent, by arranging the transistors within different cells that have the same number of transistors but different logic functions in the same geometric layout so that the cell functions cannot be determined by the transistor geometries, by using implants that are made electrically conductive by heavy doping and are not readily discernable for intracell connections, and by providing the same geometric layout of intracell interconnections for different logic cells so that the cell functions cannot be determined even if the interconnections are determined by a reverse engineer. A uniform pattern of interconnections is achieved by providing implants for all potential interconnections within each cell, and disabling unwanted interconnections for a given cell with narrow implanted channel stops of opposite conductivity. The channel stops are even more difficult to discern than are the implanted interconnections, yielding a still higher level of protection. Heavily doped implants with a common geometric layout and channel stop interruptions were also used for intercell as well as intracell connections.

The present invention retains all of these features and advantages, and in addition makes it even more difficult to detect the channel stops, and also to detect whether implanted circuit elements are electrically connected or isolated from each other even if a reverse engineer uses a selective etch that removes N and P doped areas at different etch rates.

The invention is applicable to many different kinds of digital circuits, such as various types of logic gates. Using common gates such as OR and AND gates as building blocks, many different types of logic circuitry can be designed. FIG. 1 is a schematic diagram of a conventional three-input OR gate circuit, which represents just one of the many circuits to which the invention is applicable. Three P-channel transistors 2, 4 and 6 are connected in series between a positive voltage terminal 8 and an inverted output 10, and three N-channel transistors 12, 14 and 16 are connected in parallel between a negative voltage terminal 18 (which can be designated ground) and the inverted output 10. Input terminals 20, 22 and 24 for three separate inputs are

connected to the gates of respective P-channel/N-channel transistor pairs.

The signal at inverted output 10 represents a NOR function. To convert this to an OR output, an inverter 26 inverts the signal at output 10 to produce an OR output at terminal 28. The inverter is conventional, consisting of a P-channel transistor 30 and an N-channel transistor 32 that are connected in series between the positive and negative voltage terminals 8 and 18, with the gates of transistors 30 and 32 receiving an input from inverted output 10, and output terminal 28 tapped from the series junction of transistor 30 and 32.

FIGs. 2a and 2b illustrate how the presence or absence of an electrical connection between two implanted regions of an IC can be camouflaged by making them appear the same to a reverse engineer, even if a selective etch is used.

Two heavily doped implants 34a and 34b are shown extending in from the surface of a circuit region in a semi-conductor substrate 36. The implants 34a, 34b are illustrated as being doped N+, with the substrate's circuit region lightly doped P-. One of the heavily doped conductive implants 34a, 34b could be the source or drain of a MOSFET, while the other implant could be the source or drain of an adjacent MOSFET. However, no limitation to MOSFETs is intended, and in general the implants 34a, 34b could be any conductive regions when it is desired to camouflage whether or not they are electrically connected to each other.

An electrically insulating layer 38 extends into the substrate and between the two implants 34a and 34b. Insulating layer 38 is preferably an oxide of the substrate material, and is typically formed as the field oxide resulting from a conventional local oxidation of silicon (LOCOS) process. Immediately below the insulating layer 38 is a buried layer 40 that is doped N+ and forms a conductive path between the two implants 34a and 34b. The buried layer 40 forms junctures with each of the implants, and extends upward to the juncture of the implants with the insulating layer 38 in the vicinity of the substrate surface 42. It is not necessary that the implants, buried layer 40 and insulating layer 38 meet exactly at the substrate surface; the insulating layer can extend somewhat into the lateral edge of the implants so that the buried layer does not quite reach the substrate surface, although typically the implants will be self-aligned with the insulating layer (as described below).

Although the circuit structure of FIG. 2a has N+ conductive implants set in a P- circuit region of the substrate, the invention is also applicable to a reversal of doping conductivities. In that case two P+ implants would be set in an N- substrate circuit region, and connected to each other with a P+ buried layer.

FIG. 2b illustrates the preferred structure employed by the invention when it is desired to electrically isolate two conductive implants 34a' and 34b' from each other, rather than to connect them as in FIG. 2a. An insulating layer 38', similar to insulating layer 38 of FIG. 2a, extends between the two implants 34a' and 34b'. In this case a buried layer 44 of opposite conductivity to the implants 34a' and 34b' underlies the field oxide 38' and extends between the implants. This is the usual P field implant that underlies the field oxide in the conventional LOCOS process used to isolate N+ implants from each other. The structure of FIG. 2b by itself is not new; the novelty resides in the fact that the structure of FIG. 2b has the same appearance to a reverse engineer as the structure of FIG. 2a, and therefore the reverse engineer will not be able to tell whether the N+ implants are electrically connected or electrically isolated from each other. The manner in which this camouflage works is illustrated in FIGs. 3a and 3b.

FIG. 3a illustrates the structure of FIG. 2a after a reverse engineer has removed everything above the semiconductor (typically silicon) and exposed the bare semiconductor for selective etching. Selective etching is used in reverse engineering to bring out the boundary of different diffusion or implant types at the silicon surface due to their different etch rates. With the invention, however, the removal of the field oxide 38 leaves "steps" 46a and 46b at either end of the buried connector implant 40, at the upper end of its junctures with the implants 34a and 34b in the vicinity of the substrate surface 42. These "steps" are abrupt downward slopes of the bare silicon surface relative to the substrate surface 42, and are established by the contour of the field oxide layer which has just been removed.

Field oxide grown with a LOCOS process will eat into the surface of the silicon substrate typically by an amount equal to 0.44 times the total oxide thickness. Since the field oxide thickness in a standard submicron CMOS process is about 0.5 micrometer (micron), after removing the field oxide and exposing the bare silicon surface the steps 46a and 46b at the edge of the removed field oxide will be about 0.2 microns deep. However, the junction depth of all implants with submicron CMOS processes is normally about 0.2-0.3 microns (except for the P or N well junction). Any difference in etch rate between the P field implant 44 and the buried conductive layer implant 40 will therefore be less than 0.2-0.3 microns, and will be masked by the existing step of about 0.2 microns established by the field oxide.

The substrate depth after a selective etch which removes N-doped material at a faster rate than P-doped material is illustrated in FIG. 3a by dashed lines, with dashed line 48 representing the surface of the P- substrate circuit region, and dashed line 50 the surface of the N+ implants and buried layer. After the etch has been completed the steps 52a and 52b at the facing edges of the remainder of N+ implants 34a and 34b have a slope and depth that is still influenced mostly by the slope and depth of the original steps 46a and 46b as they existed prior to the etch.

FIG. 3b illustrates the results of selective etching for the electrically isolating P field buried layer 44. The

steps 46a' and 46b' at the edges of N+ implants 34a' and 34b' prior to etching are essentially equal in slope and depth to the steps 46a and 46b for the conductive buried layer 40 of FIG. 3a, and the dashed line 48' representing the post-etch surface of the P- circuit region is also essentially the same as dashed line surface 48. However, the post-etch surface of the P field implant (indicated by dashed line 50') is somewhat shallower than the post-etch surface 50 of the N+ conductive buried layer in FIG. 3a. This results in post-etch steps 52a' and 52b' that are not quite as deep as the post-etch steps 52a and 52b. This difference in post-etch step depths is less than what would normally be expected from the selective nature of the etchant, since the upper edges of steps 52a and 52b are established by the relatively large etch depths of the N+ material in implants 34a and 34b, whereas the upper edges of post-etch steps 52a' and 52b' are established by the relatively lesser depth of the P field etch and are thus higher than for steps 52a and 52b. The result is that after selective etching there will not be any obviously different trace, along the boundaries of the area underlying the removed field oxide, between the N+ buried channel implant 40 and the P field implant 44. Any difference will be slight enough that the presence of an N+ buried connector layer instead of the usual P field implant cannot be detected by either an optical microscope or an SEM after selective etching.

FIGs. 4-7 illustrate the application of the invention to MOSFET transistors formed on a semiconductor substrate 54. The substrate is illustrated as having a primary P-doping conductivity, with N-channel MOSFETs T1 and T2 formed directly in the bulk of the substrate, and a pair of P-channel MOSFETs T3 and T4 formed within a circuit region established by an N- well 56 in the substrate. Transistors T1, T2, T3 and T4 have respective sources S1, S2, S3 and S4, drains D1, D2, D3 and D4, and polysilicon gates G1, G2, G3 and G4 overlying transistor channels between their respective sources and drains. Transistors T1 and T2 are adjacent to each other, as are transistors T3 and T4. In conventional, uncamouflaged circuits any connections between T1 and T2 and between T3 and T4 would be made by upper metalization layers, and would thus be readily apparent to a reverse engineer. Each transistor would be entirely surrounded by field oxide, which would isolate the adjacent transistors from each other through the substrate and allow for connections between them only through the metalization.

The transistors T1 and T2 are separated by a central region C, which extends between the central portions of D1 and S2 and is bounded laterally by regions A and B extending between the lateral portions of D1 and S2 on opposite sides of region C. Region C is covered with a field oxide layer, with either a buried conductive N+ layer electrically connecting D1 and S2 below the field oxide, or a buried P field implant isolating D1 from S2 below the field oxide. The substrate surface in regions A and B is bare, with no field oxide. Regions A and B have the same P field implant, whether or not a conductive N+ buried layer is provided in region C. Any electrical connection between D1 and S2 is therefore restricted to region C. The remainder of the surface of substrate 54 surrounding the transistors has the usual field oxide and underlying P field implant.

Since region C has a field oxide layer but all of the regions bounding it (A, B, D1 and S2) are without field oxide layers, steps are formed around the entire boundary of region C. These steps camouflage the nature of the doped layer below the field oxide and prevent a reverse engineer from determining whether it is a conductive N+ buried layer or an insulative P field implant, as described above.

The structure provided for P-channel transistors T3 and T4 is similar to that for T1 and T2, but with reverse conductivities. A central region F between D3 and S4 is covered with field oxide, with a buried P+ layer below the field oxide providing any conductive path between D3 and S4. Region F is laterally bounded by regions D and E, which are without field oxide layers and have N field implants which do not provide any conductive path between D3 and S4.

While in FIG. 4 the drain of one transistor is shown as being connectable to the source of its paired transistor, the transistor layouts could be rearranged to provide camouflaged connections between both sources or both drains. As shown in FIG. 4, the two P-channel transistors T3 and T4 could correspond to transistors 2 and 4 of FIG. 1, with the drain of transistor 2 connected to the source of transistor 4. By rearranging these transistors to have their sources face each other, T3 and T4 could correspond respectively to transistors 2 and 30 of FIG. 1, which have their sources connected together. Similarly, rearranging T1 and T2 so that either their sources or their drains faced each other would allow these transistors to correspond to parallel-connected N-channel transistors 12 and 14 in FIG. 1.

FIG. 5 is a sectional view through region A of FIG. 4; a sectional view through region B would look the same. In region A a P field implant 58 extends between D1 and S2. A common field oxide layer 60 and underlying P field implant 62 surround the outer transistor edges.

FIG. 6 shows region C between transistors T1 and T2, including a field oxide layer 64 extending between D1 and S2. FIG. 6 illustrates the case of an N+ buried layer 66 underlying the field oxide 64 and providing an electrical connection between D1 and S2, as in FIG. 2a. A P field implant, below field oxide 64, as in FIG. 2b, would together with the field oxide inhibit current flow between D1 and S2.

FIG. 7 shows a sectional view through region C taken at right angles to the view of FIG. 6. From FIG. 7 it can be seen that the field oxide 64 in region C forms steps with respect to the substrate surface at its boundaries with the P field implant 62, which extends up to the

substrate surface in regions A and B since no field oxide is present in these regions. From FIG. 6 it can be seen that the region C field oxide 64 forms steps with respect to the substrate surface at its boundaries with D1 and S2. Thus, region C is completely bounded by steps which camouflage the presence or absence of an N+ buried conductive layer connecting D1 with S2.

Although region C is shown as a single region that is symmetrically positioned with respect to the transistors T1 and T2, other configurations could be employed as long as the regions through which any connections are made between D1 and S2 are bounded by steps in the substrate to inhibit reverse engineering. For example, region C could be divided into multiple areas, each with a field oxide and mutually separated by P field implants without field oxides. Region C could also be extended along the full widths of the transistors if the field oxide is removed from the immediately adjacent portions of the substrate surrounding the transistors.

FIG. 8 is a sectional view through region F and transistors T3 and T4, showing the similar structure for the P-channel transistors. A field oxide 68 is formed in region F, with either a buried conductive P+ implant 70 connecting D3 and S4 below the field oxide, or an N field implant (not shown) that cooperates with field oxide 68 to inhibit current flow between D3 and S4. An N field implant 70 is provided below the field oxide layer 72 in the N-well 56 surrounding T3 and T4.

The preferred sequence to fabricate the IC structure described above is to first form a mask on the substrate surface, typically consisting of a layer of Si_3N_4 over a layer of SiO_2, to expose the field implant areas. The field implants which underlie the later conventional field oxide layer and also establish the regions A, B, D and E of FIG. 4 are then performed; boron is typically used for a P field implant for regions A and B, and arsenic or phosphorous for an N field implant for regions D and E. The implants are preferably performed with a flood beam, although older diffusion techniques or a focused ion beam could also be used. The field implants are typically made to a depth of about 0.2 to 0.6 microns, with a dopant concentration on the order of 10^{18} atoms/cm^3 or higher.

After the field implants have been completed, a new mask is laid down to expose the areas intended for the buried conductive layers, such as layer 66 in FIG. 6 or 70 in FIG. 8. The conductive layers are then implanted, typically to a depth of about 0.5 to 2.0 microns and a doping concentration on the order of 10^{19} atoms/cm^3 or higher. The regions C and F of FIG. 4 would be implanted at this time if conductive interconnects between their respective transistors are desired; blocking field implants would have been provided in the previous implant step if interconnections were not desired. For both the blocking field implants and the conductive buried layer implants, separate masks would be provided and separate implants performed for the N-channel and P-channel devices.

The field oxide layers are next grown using a standard LOCOS process, followed by the formation of thin gate oxide layers (typically about 100-150 Angstroms thick for a 0.5 micron channel length) over the transistor areas exposed by the field oxide, and then the deposit of polysilicon over the entire substrate surface and an etch removal of the polysilicon except from the desired gate areas. Finally, source and drain implants are performed using the field oxide and gates as masks so that they are self-aligned with the source and drain implants. A separate mask would be provided over areas A, B, D and E of FIG. 4 to prevent the dopant from penetrating the substrate in these areas.

To reduce any disruption of the standard CMOS fabrication process, the insulative field implants and conductive buried layer implants associated with the new camouflage technique are preferably performed after the well drive-in and before the growth of field oxide to prevent the high-temperatures associated with the well drive-in from affecting the concentration profile of the dopant implants.

The insulative field implant has a doping concentration that is higher than the doping concentration of the bulk of the substrate or the well in which it is set, but less than the source and drain doping concentration. With the substrate bulk and well having a doping concentration on the order of 10^{15} to 10^{16} atoms/cm^3 and the source/drain implants having a doping concentration on the order of 10^{19} to 10^{20} atoms/cm^3, a typical field implant concentration of about 10^{18} atoms/cm^3 produces an overall resistivity that is roughly five times greater than the resistivity of the source/drain implants (the resistivity will actually vary over the volume of the implants, since the doping concentrations are typically lighter towards the bottoms of the implants than towards their tops). This concentration differential prevents an excessive reduction in the breakdown voltage between the two adjacent transistors, and allows the field implants to perform an insulating function between adjacent transistors.

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Such variations and alternate embodiments are contemplated, and can be made without departing from the spirit and scope of the invention as defined in the appended claims.

The present invention discloses a camouflaged circuit structure, wherein connections between implanted regions 34a, 34b in a semiconductor substrate 36, such as the sources S1, S2 or drains D1, D2 of adjacent transistors T1, T2, are made by buried conductive implants 40 rather than upper level metalizations. The presence or absence of a connection between two implanted regions is camouflaged by implanting a conductive buried layer 40 of the same doping conductivity as the implanted regions when a connection is desired, and a field implant 44 of opposite conductivity to the implanted

regions when no connection is desired, and forming steps 46a, 46b into the substrate at the boundaries of the buried layer or field implant that mask the steps 52a, 52b formed between different conductivity regions during a selective etch by a reverse engineer. The masking steps are preferably formed by field oxide layers 38 that terminate at the boundaries of the buried layers and field implants.

Claims

1. A camouflaged circuit structure, comprising:

   a semiconductor substrate (36), and
   a first pair of spaced conductive implants (34a, 34b) having a common conductivity and extending into said substrate (36),
   characterized by
   a first electrically insulating layer (38) extending into said substrate between said conductive implants, and
   a conductive first buried layer (40) of the same conductivity as said spaced conductive implants disposed within said substrate immediately below said electrically insulating layer and electrically connecting said spaced conductive implants (34a, 34b).

2. The circuit structure of claim 1, characterized in that said substrate has a surface (42) into which said implants (34a, 34b) and electrically insulating layer (38) extend, said electrically insulating layer (38) forming respective steps (46a, 46b), relative to said surface, in the vicinity of said conductive implants (34a, 34b).

3. The circuit structure of claims 1 or 2, characterized in that said electrically insulating layer (38) comprises an oxide of the substrate material.

4. The circuit structure of any of claims 1-3, characterized in that one of said conductive implants (34a, 34b) comprises a source (S1) or drain (D1) of a metal-oxide-semiconductor field effect transistor (MOSFET) (T1), and the other of said conductive implants (34a, 34b) comprises a source (S2) or drain (D2) of another MOSFET (T2).

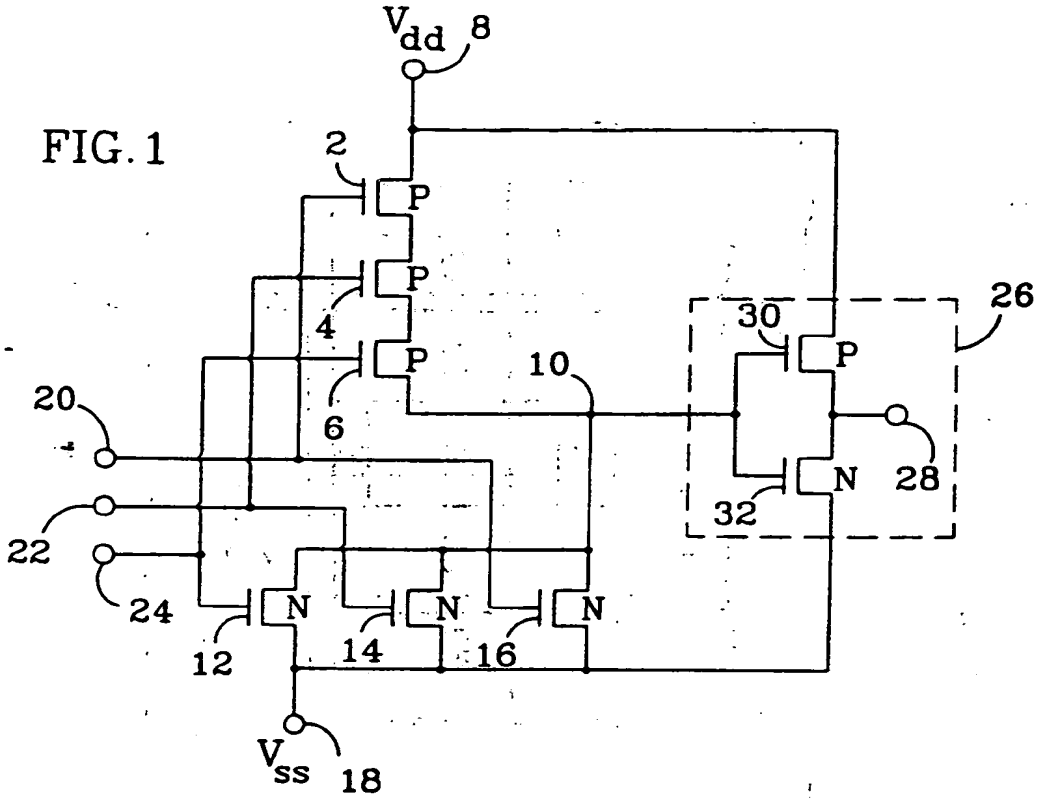
5. The circuit structure of any of claims 1-4, characterized by a second pair of spaced conductive implants (34a', 34b') with the same conductivity as said first pair (34a, 34b) and extending into said substrate (36), a second electrically insulating layer (38') extending into said substrate between said second pair of conductive implants (34a', 34b'), and a second buried layer (44), doped opposite to the conductivity of said second pair of implants (34a', 34b'), disposed within said substrate (36) immediately below said second electrically insulating layer (38') and extending between said second pair of implants (34a', 34b'), said second insulating layer (38') together with said second buried layer (44) inhibiting current flow between said second pair of implants (34a', 34b').

6. The circuit structure of any of claims 1-5, characterized in that said substrate (36) is doped to a primary substrate conductivity, and said implants (34a, 34b; 34a', 34b') are doped opposite to said primary substrate conductivity.

7. The circuit structure of any of claims 1-5, characterized in that said substrate (36) is doped to a primary substrate conductivity, and said implants (34a, 34b; 34a', 34b') are doped to the same conductivity as said primary substrate conductivity and set in a substrate well (56) doped opposite to said primary substrate conductivity.

8. The circuit structure of any of claims 1-4 or 6, characterized by a second pair of spaced conductive implants (D3, S4) of opposite conductivity to said first pair (34a, 34b) and extending into said substrate (36), a second insulating layer (68) extending into said substrate (36) between said second pair of implants, and a second doped buried layer (70) disposed within said substrate (36) immediately below said second electrically insulating layer (68) and extending between said second pair of implants (34a', 34b'), said substrate (36) being doped to a primary substrate conductivity, and one of said pairs of implants and their associated insulating layer and buried layer being set in a doped substrate well (56) of opposite conductivity to said primary substrate conductivity.

FIG. 1



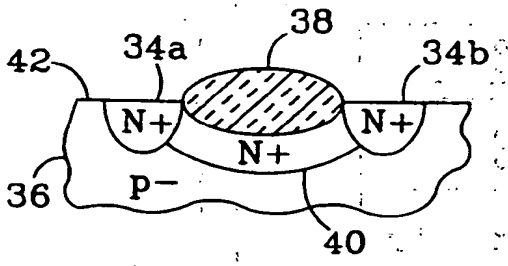


FIG. 2a

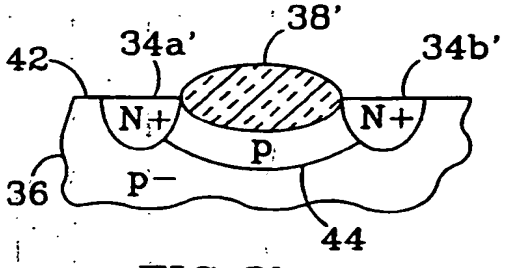


FIG. 2b

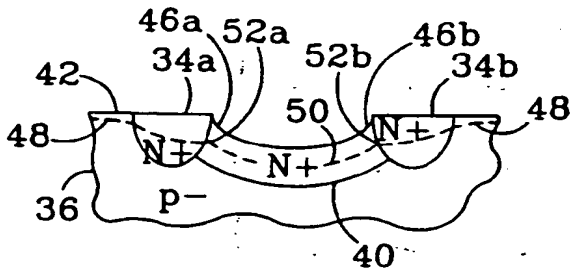


FIG. 3a

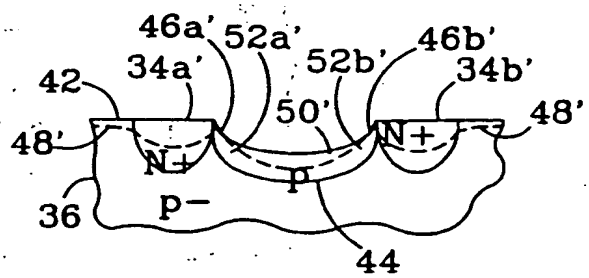


FIG. 3b

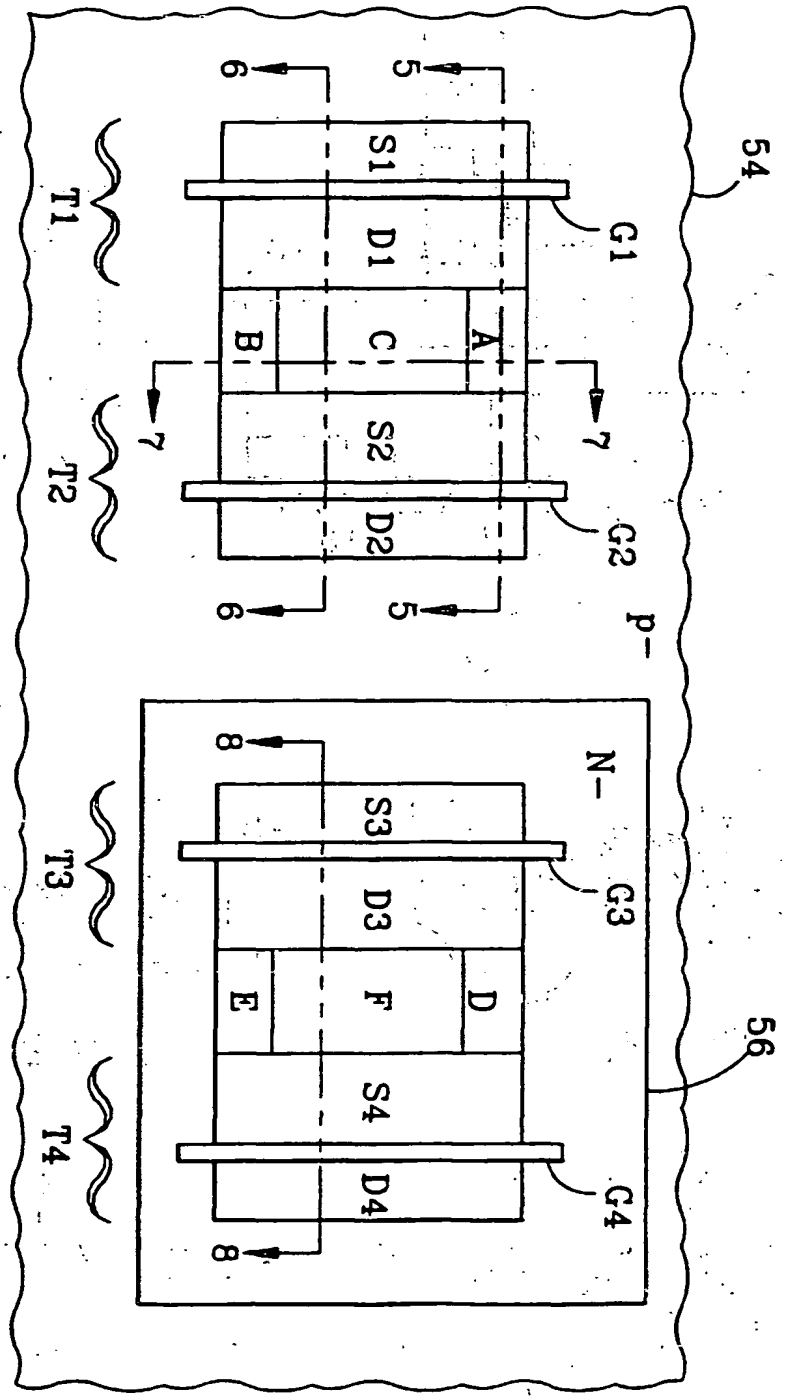


FIG.4

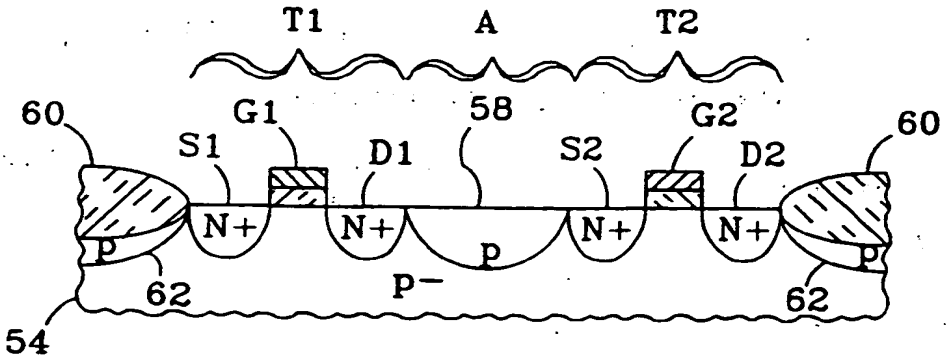


FIG.5

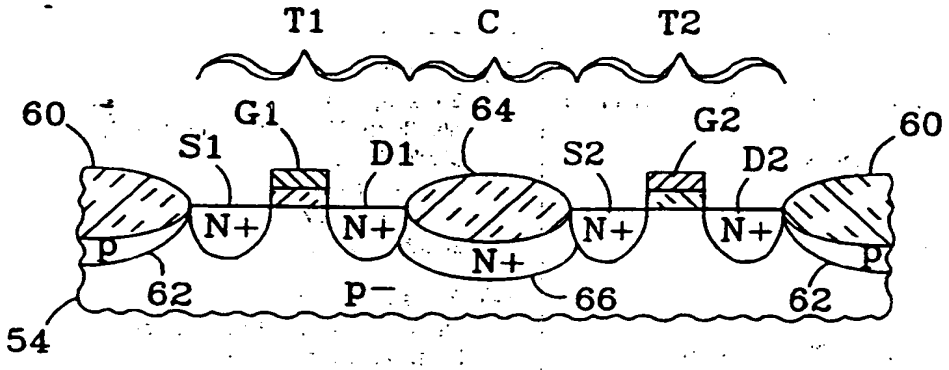


FIG.6

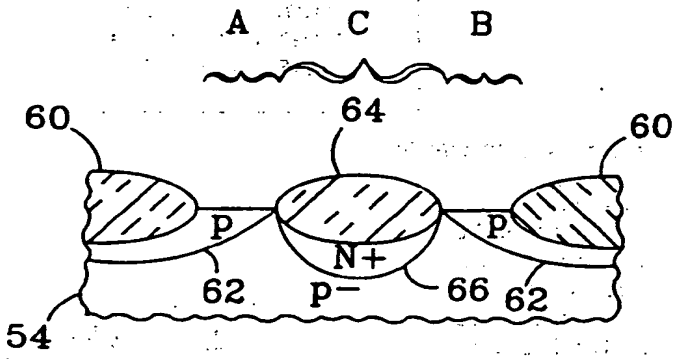


FIG.7

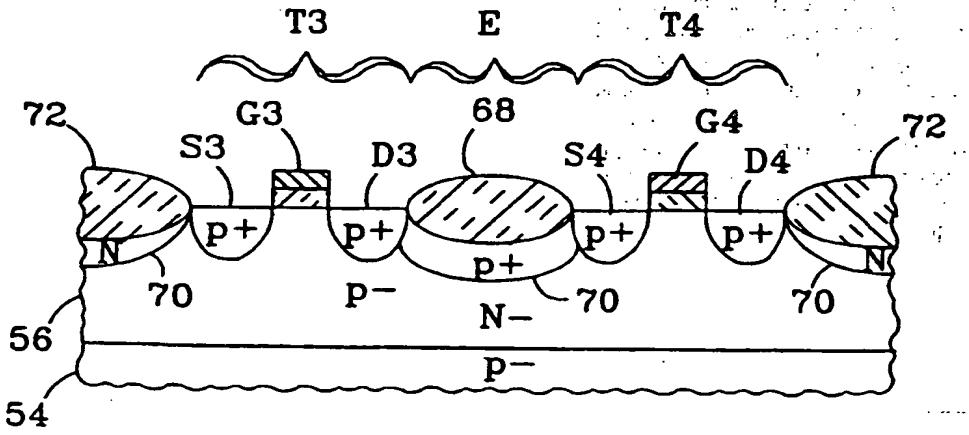


FIG.8

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(54) Camouflaged circuit structure with implants

(57) Connections between implanted regions (34a, 34b) in a semiconductor substrate (36), such as the sources (S1, S2) or drains (D1, D2) of adjacent transistors (T1, T2), are made by buried conductive implants (40) rather than upper level metalizations. The presence or absence of a connection between two implanted regions is camouflaged by implanting a conductive buried layer (40) of the same doping conductivity as the implanted regions when a connection is desired, and a field implant (44) of opposite conductivity to the implanted regions when no connection is desired, and forming steps (46a, 46b) into the substrate at the boundaries of the buried layer or field implant that mask the steps (52a, 52b) formed between different conductivity regions during a selective etch by a reverse engineer. The masking steps are preferably formed by field oxide layers (38) that terminate at the boundaries of the buried layers and field implants.

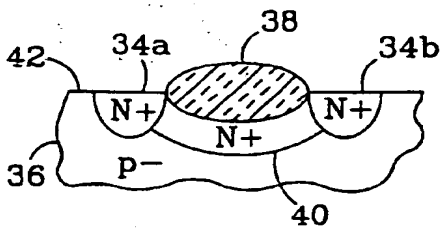

FIG.2a

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EUROPEAN SEARCH REPORT

Application Number
EP 98 10 9940

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 4 101 344 A (KOOI ELSE ET AL) 18 July 1978 (1978-07-18) * column 2, line 25 - column 9, line 17; figures 1-11 *	1-8	H01L27/02 H01L21/74 H01L23/535
X	US 4 374 454 A (JOCHEMS PIETER J W) 22 February 1983 (1983-02-22) * column 4, line 21 - column 10, line 41; figures 1-13 *	1-8	
X	US 4 343 079 A (JOCHEMS PIETER J W) 10 August 1982 (1982-08-10) * column 5, line 8 - column 9, line 35; figures 1-11 *	1-8	
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 550 (E-1009), 6 December 1990 (1990-12-06) & JP 02 237038 A (RICOH CO LTD), 19 September 1990 (1990-09-19) * abstract *	1-8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
Y	PATENT ABSTRACTS OF JAPAN vol. 018, no. 049 (E-1497), 26 January 1994 (1994-01-26) & JP 05 275529 A (MATSUSHITA ELECTRON CORP), 22 October 1993 (1993-10-22) * abstract *	1-8	H01L
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 105 (E-1512), 21 February 1994 (1994-02-21) & JP 05 304207 A (OKI ELECTRIC IND CO LTD), 16 November 1993 (1993-11-16) * abstract *	1-8	
	-/--		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	25 October 1999	Berthold, K

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E : earlier patent document, but published on, or after the filing date
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Application Number
EP 98 10 9940

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 585 601 A (HUGHES AIRCRAFT CO) 9 March 1994 (1994-03-09) * abstract; figures 3A,3B *	1-8	
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 088 (E-240), 21 April 1984 (1984-04-21) & JP 59 008352 A (NIPPON GAKKI SEIZO KK), 17 January 1984 (1984-01-17) * abstract *	5,7,8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	25 October 1999	Berthold, K

CATEGORY OF CITED DOCUMENTS

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25-10-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4101344 A	18-07-1978	NL 7611773 A	27-04-1978
		AU 506465 B	03-01-1980
		AU 2090876 A	29-06-1978
		CA 1075372 A	08-04-1980
		CH 623959 A	30-06-1981
		DE 2745857 A	27-04-1978
		FR 2368799 A	19-05-1978
		GB 1567197 A	14-05-1980
		IT 1066832 B	12-03-1985
		JP 1358815 C	13-01-1987
		JP 53053276 A	15-05-1978
		JP 61012382 B	08-04-1986
		SE 414980 B	25-08-1980
		SE 7614157 A	26-04-1978
US 4374454 A	22-02-1983	NL 8003612 A	18-01-1982
		AU 545453 B	18-07-1985
		AU 7203181 A	07-01-1982
		CA 1163378 A	06-03-1984
		EP 0042643 A	30-12-1981
		IE 51994 B	13-05-1987
		JP 1400251 C	28-09-1987
		JP 57031180 A	19-02-1982
		JP 62002708 B	21-01-1987
US 4343079 A	10-08-1982	NL 7903158 A	27-10-1980
		AU 537858 B	19-07-1984
		AU 5765180 A	30-10-1980
		CA 1146675 A	17-05-1983
		CH 653482 A	31-12-1985
		DE 3015101 A	06-11-1980
		FR 2455361 A	21-11-1980
		GB 2047961 A,B	03-12-1980
		JP 55141758 A	05-11-1980
JP 02237038 A	19-09-1990	NONE	
JP 05275529 A	22-10-1993	NONE	
JP 05304207 A	16-11-1993	NONE	
EP 0585601 A	09-03-1994	DE 69324637 D	02-06-1999
		EP 0940851 A	08-09-1999
		IL 106513 A	18-03-1997
		JP 6163539 A	10-06-1994
		US 5866933 A	02-02-1999

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 59008352 A	17-01-1984	NONE	

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